

# 74LVCH32245A

32-bit bus transceiver with direction pin; 5 V tolerant; 3-state

Rev. 03 — 20 August 2007

Product data sheet

## 1. General description

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The 74LVCH32245A is a 32-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The device features four output enable ( $n\overline{OE}$ ) inputs for easy cascading and four send/receive ( $n\overline{DIR}$ ) inputs for direction control. Pin  $n\overline{OE}$  controls the outputs so that the buses are effectively isolated.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

To ensure the high-impedance state during power-up or power-down, pin  $n\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

## 2. Features

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- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- High-impedance when  $V_{CC} = 0$  V
- All data inputs have bus hold
- Complies with JEDEC standard JESD8-B / JESD36
- ESD protection:
  - ◆ HBM EIA/JESD22-A114-B exceeds 2000 V
  - ◆ MM EIA/JESD22-A115-A exceeds 200 V
- Specified from  $-40$  °C to  $+85$  °C
- Packaged in plastic fine-pitch ball grid array package

### 3. Ordering information

**Table 1. Ordering information**

Type number	Package			
	Temperature range	Name	Description	Version
74LVCH32245AEC	-40 °C to +85 °C	LFBGA96	plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm	SOT536-1

4. Functional diagram

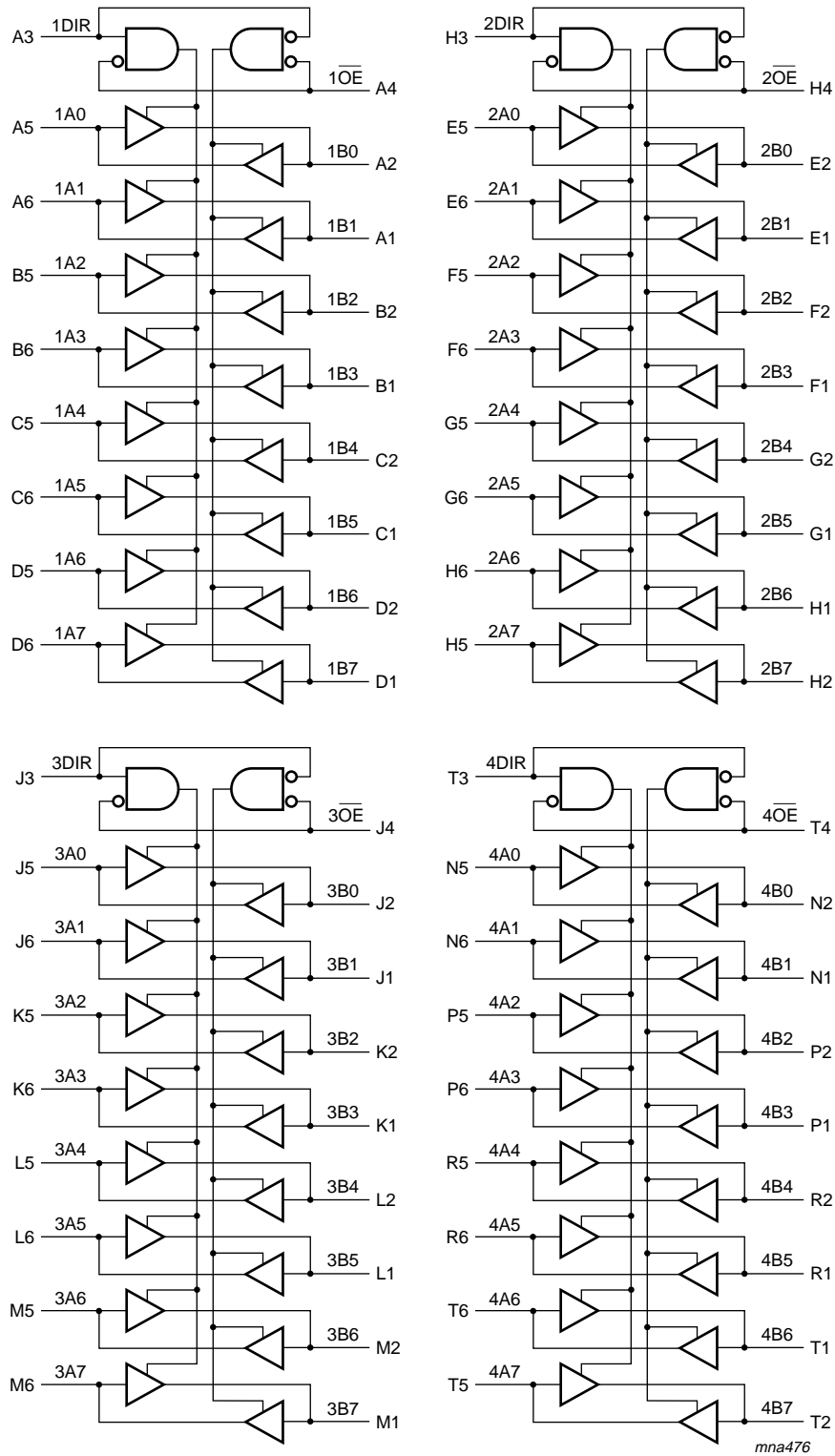


Fig 1. Logic symbol

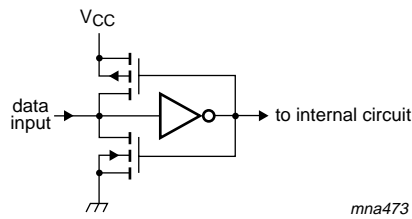


Fig 2. Bus hold circuit

## 5. Pinning information

### 5.1 Pinning

*mna475*

6	1A1	1A3	1A5	1A7	2A1	2A3	2A5	2A6	3A1	3A3	3A5	3A7	4A1	4A3	4A5	4A6
5	1A0	1A2	1A4	1A6	2A0	2A2	2A4	2A7	3A0	3A2	3A4	3A6	4A0	4A2	4A4	4A7
4	1 $\overline{OE}$	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	2 $\overline{OE}$	3 $\overline{OE}$	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	4 $\overline{OE}$
3	1DIR	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	2DIR	3DIR	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	4DIR
2	1B0	1B2	1B4	1B6	2B0	2B2	2B4	2B7	3B0	3B2	3B4	3B6	4B0	4B2	4B4	4B7
1	1B1	1B3	1B5	1B7	2B1	2B3	2B5	2B6	3B1	3B3	3B5	3B7	4B1	4B3	4B5	4B6
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

Fig 3. Pin configuration

### 5.2 Pin description

Table 2. Pin description

Pin name	Ball	Description
nDIR (n = 1 to 4)	A3, H3, J3, T3	direction control
n $\overline{OE}$ (n = 1 to 4)	A4, H4, J4, T4	output enable input (active LOW)
1A[0:7]	A5, A6, B5, B6, C5, C6, D5, D6	input or output
1B[0:7]	A2, A1, B2, B1, C2, C1, D2, D1	input or output
2A[0:7]	E5, E6, F5, F6, G5, G6, H6, H5	input or output
2B[0:7]	E2, E1, F2, F1, G2, G1, H1, H2	input or output
3A[0:7]	J5, J6, K5, K6, L5, L6, M5, M6	input or output
3B[0:7]	J2, J1, K2, K1, L2, L1, M2, M1	input or output
4A[0:7]	N5, N6, P5, P6, R5, R6, T6, T5	input or output
4B[0:7]	N2, N1, P2, P1, R2, R1, T1, T2	input or output
GND	B3, B4, D3, D4, E3, E4, G3, G4, K3, K4, M3, M4, N3, N4, R3, R4	ground (0 V)
V <sub>CC</sub>	C3, C4, F3, F4, L3, L4, P3, P4	supply voltage

## 6. Functional description

Table 3. Function selection<sup>[1]</sup>

Input		Output		
nOE	nDIR	nAn	nBn	
L	L	A = B	inputs	
L	H	inputs	B = A	
H	X	Z	Z	

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
V <sub>I</sub>	input voltage		[1] -0.5	+6.5	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0 V	-	±50	mA
V <sub>O</sub>	output voltage	output HIGH or LOW state	[2] -0.5	V <sub>CC</sub> + 0.5	V
		output 3-state	[2] -0.5	+6.5	V
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub>	supply current		[3] -	200	mA
I <sub>GND</sub>	ground current		[3] -200	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +85 °C	[4] -	1000	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] All supply and ground pins connected externally to one voltage source.

[4] Above 70 °C the value of P<sub>tot</sub> derates linearly with 1.8 mW/K.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage	for maximum speed performance	2.7	-	3.6	V
		for low-voltage applications	1.2	-	-	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage	output HIGH or LOW state	0	-	V <sub>CC</sub>	V
		output 3-state	0	-	5.5	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.2 V to 2.7 V	-	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	Min	Typ <sup>[1]</sup>	Max	Unit	
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>								
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	-	-	V	
			2.7 to 3.6	2.0	-	-	V	
V <sub>IL</sub>	LOW-level input voltage		1.2	-	-	GND	V	
			2.7 to 3.6	-	-	0.8	V	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
			I <sub>O</sub> = -100 μA	2.7 to 3.6	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V
			I <sub>O</sub> = -12 mA	2.7	V <sub>CC</sub> - 0.5	-	-	V
			I <sub>O</sub> = -18 mA	3.0	V <sub>CC</sub> - 0.6	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
			I <sub>O</sub> = 100 μA	2.7 to 3.6	-	GND	0.20	V
			I <sub>O</sub> = 12 mA	2.7	-	-	0.40	V
			I <sub>O</sub> = 24 mA	3.0	-	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	<a href="#">[2]</a>	±0.1	±5	μA	
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND	3.6	<a href="#">[2]</a> <a href="#">[3]</a>	±0.1	±5	μA	
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	-	±0.1	±10	μA	
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	3.6	-	0.1	40	μA	
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	2.7 to 3.6	-	5	500	μA	
C <sub>I</sub>	input capacitance	V <sub>I</sub> = GND to V <sub>CC</sub>	0 to 3.6	-	5.0	-	pF	
C <sub>I/O</sub>	input/output capacitance	V <sub>I</sub> = GND to V <sub>CC</sub>	0 to 3.6	-	10	-	pF	
I <sub>BHL</sub>	bus hold LOW current	V <sub>I</sub> = 0.8 V	3.0	<a href="#">[4]</a> <a href="#">[5]</a>	75	-	μA	
I <sub>BHH</sub>	bus hold HIGH current	V <sub>I</sub> = 2.0 V	3.0	<a href="#">[4]</a> <a href="#">[5]</a>	-75	-	μA	
I <sub>BHLO</sub>	bus hold LOW overdrive current		3.6	<a href="#">[4]</a> <a href="#">[6]</a>	500	-	μA	
I <sub>BHHO</sub>	bus hold HIGH overdrive current		3.6	<a href="#">[4]</a> <a href="#">[6]</a>	-500	-	μA	

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

[2] The bus hold circuit is switched off when V<sub>I</sub> > V<sub>CC</sub> allowing 5.5 V on the input terminal.

[3] For I/O ports the parameter I<sub>OZ</sub> includes the input leakage current.

[4] Valid for data inputs only. Note that control inputs do not have a bus hold circuit.

[5] The specified sustaining current at the data input holds the input below the specified V<sub>I</sub> level.

[6] The specified overdrive current at the data input forces the data input to the opposite input state.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 6](#).

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	Min	Typ <sup>[1]</sup>	Max	Unit	
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>								
t <sub>pd</sub>	propagation delay	nAn to nBn; nBn to nAn; see <a href="#">Figure 4</a>	1.2	[2]	-	13.0	-	ns
			2.7		1.0	2.7	4.7	ns
			3.0 to 3.6		1.0	2.2	4.5	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn, nBn; see <a href="#">Figure 5</a>	1.2	[2]	-	15.0	-	ns
			2.7		1.5	3.6	6.7	ns
			3.0 to 3.6		1.0	2.8	5.5	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn, nBn; see <a href="#">Figure 5</a>	1.2	[2]	-	11.0	-	ns
			2.7		1.5	3.4	6.6	ns
			3.0 to 3.6		1.5	3.2	5.6	ns
t <sub>sk(o)</sub>	output skew time		3.0 to 3.6	[3]	-	-	1.0	ns
C <sub>PD</sub>	power dissipation capacitance	per buffer; V <sub>I</sub> = GND to V <sub>CC</sub>	3.3	[4]	-	30	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.2 V, 2.7 V, and 3.3 V respectively.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.  
 t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.  
 t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz

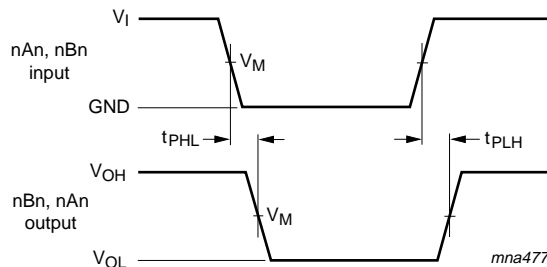
C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

## 11. Waveforms

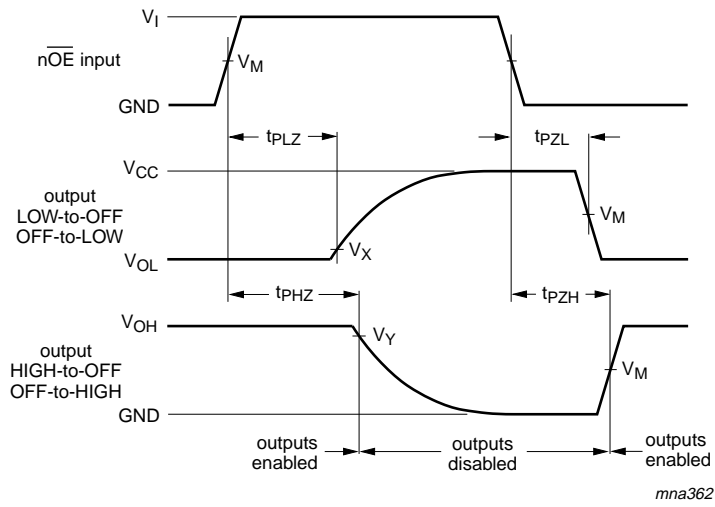


V<sub>M</sub> = 1.5 V at V<sub>CC</sub> ≥ 2.7 V.

V<sub>M</sub> = 0.5 × V<sub>CC</sub> at V<sub>CC</sub> < 2.7 V.

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage levels that occur with the output load.

**Fig 4. The input (nAn, nBn) to output (nBn, nAn) propagation delays**



$V_M = 1.5 \text{ V}$  at  $V_{CC} \geq 2.7 \text{ V}$ .

$V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7 \text{ V}$ .

$V_X = V_{OL} + 0.3 \text{ V}$  at  $V_{CC} \geq 2.7 \text{ V}$ ;

$V_X = V_{OL} + 0.15 \text{ V}$  at  $V_{CC} < 2.7 \text{ V}$ .

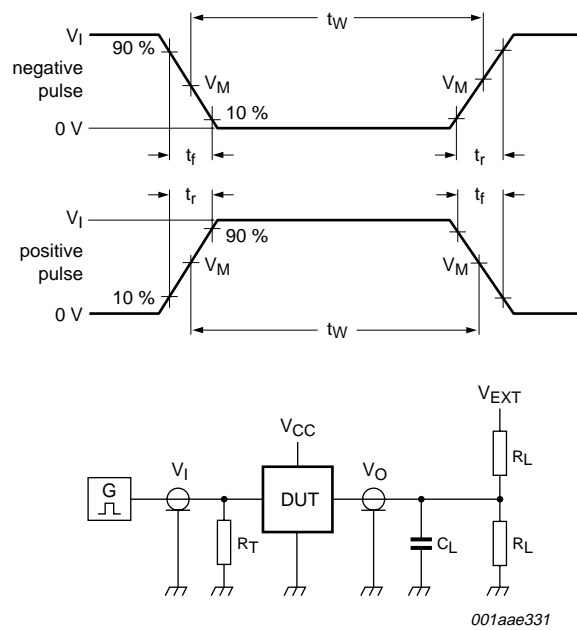
$V_Y = V_{OH} - 0.3 \text{ V}$  at  $V_{CC} \geq 2.7 \text{ V}$ ;

$V_Y = V_{OH} - 0.15 \text{ V}$  at  $V_{CC} < 2.7 \text{ V}$ .

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 5. 3-state enable and disable times.**





Test data is given in [Table 8](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 6. Load circuitry for switching times**

**Table 8. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.2 V	$V_{CC}$	$\leq 2$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND

12. Package outline

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1

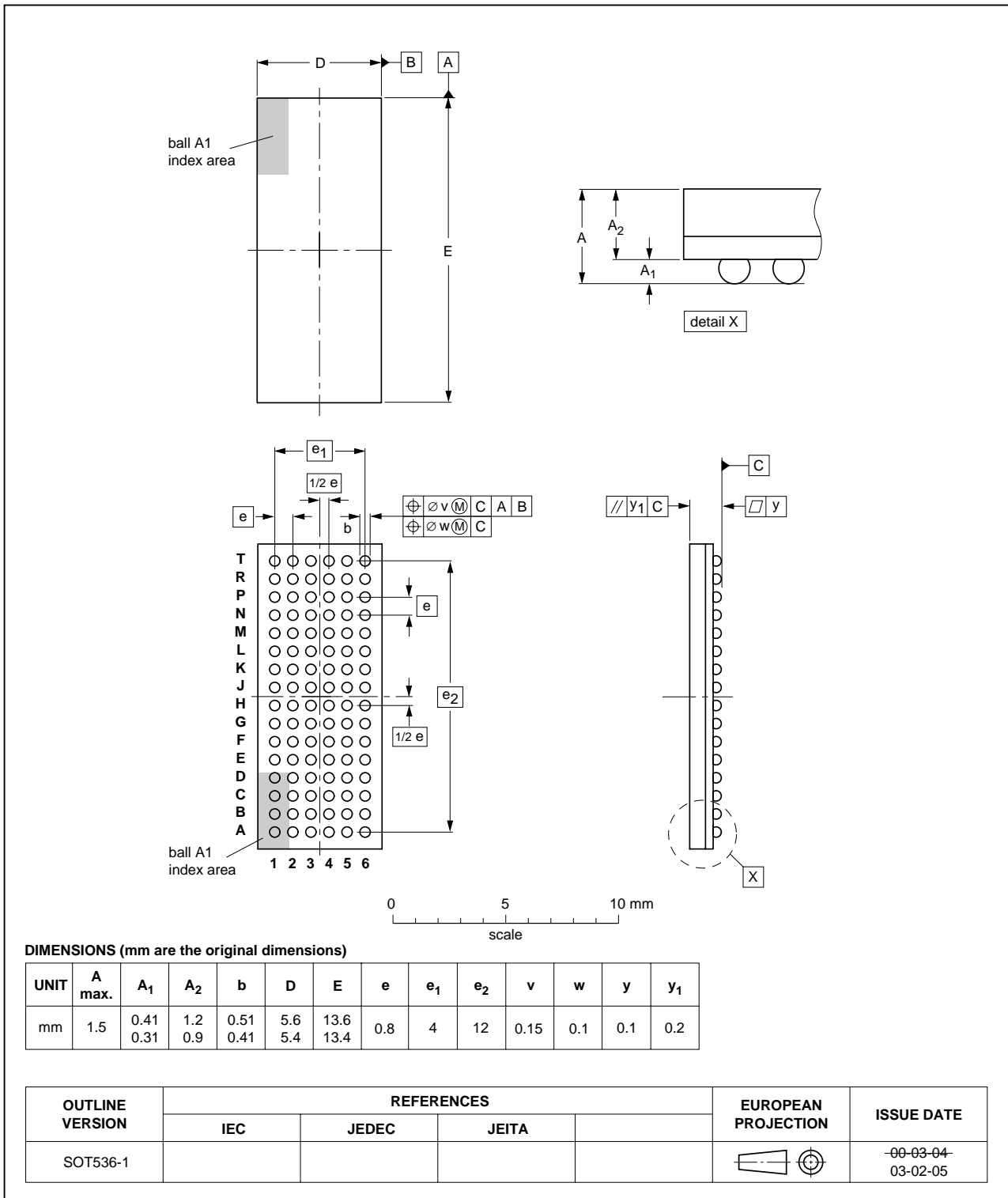


Fig 7. Package outline SOT536-1 (LFBGA96)

## 13. Abbreviations

**Table 9. Abbreviations**

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

**Table 10. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVCH32245A_3	20070820	Product data sheet	-	74LVCH32245A_2
	Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Error in <a href="#">Table 2 "Pin description"</a> corrected.</li> <li>Quick Reference Data section deleted. Information (<math>C_{PD}</math>, <math>C_I</math>, <math>C_{I/O}</math>) moved from it to <a href="#">Table 6</a> and <a href="#">Table 7</a>.</li> <li>Some parameter symbols and descriptions have been updated to comply with NXP guidelines.</li> </ul>		
74LVCH32245A_2	20040511	Product specification	-	74LVC_LVCH32245A_1
74LVC_LVCH32245A_1	19990901	-	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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